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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/571,142	11/22/2006	Kenshi Fukumitsu	46884-5461	3680

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DRINKER BIDDLE & REATH (DC)
1500 K STREET, N.W.
SUITE 1100
WASHINGTON, DC 20005-1209

EXAMINER	
WHALEN, DANIEL B	
ART UNIT	PAPER NUMBER
2829	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/571,142	FUKUMITSU ET AL.	
	Examiner	Art Unit	
	DANIEL WHALEN	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03/09/2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 9-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurosawa et al. (US 6,756,562 B1; hereinafter "Kurosawa") in view of Kajiyama et al. (US 2004/0266138 A1) and Swada (US 2002/0115235 A1).

3. **Re Claim 9**, Kurosawa teaches a semiconductor substrate cutting method for cutting a semiconductor substrate having a front face formed with a plurality of functional devices into the individual functional devices, so as to manufacture a semiconductor device having the functional device, the method comprising the steps of:

attaching a protective member (22) to the front face (21A) of the semiconductor substrate (21), such that the functional devices (21-1,21-2,21-3) are covered (fig. 16);

irradiating the semiconductor substrate with laser light (29) while position a light – converging point (point where the light converges) within the semiconductor substrate with a rear face (21B) of the semiconductor substrate acting as a laser light incidence face after attaching the protective member (fig. 21), so as to form a modified region (30A-1,30A-2,30A-3), and causing the modified region to form a starting point region (col. 4, lines 64-67) for cutting along each line along which the semiconductor substrate

should be cut, the lines set like a grid running (fig. 21, dotted lines) between the neighboring functional devices, inside by a predetermined distance from the laser light incidence face (fig. 21, see distance from the rear surface and the modified regions);

attaching an expandable holding member (26) to the rear face (21B) of the semiconductor substrate after forming the starting point regions for cutting (fig. 21, 26); and

cutting the semiconductor substrate into a plurality of semiconductor chips from the starting point regions for cutting along each of the lines in the grid (fig. 25-26).

However, Kurosawa does not disclose attaching an expandable holding member is by way of a die bonding resin layer; cutting the die bonding resin layer along each of cut surfaces of the semiconductor chips by expanding the holding member after attaching the holding member, so as to obtain the semiconductor chips each having the front face formed with the function device and having a cut piece of the die bonding resin layer in close contact with the rear face thereof; and mounting the semiconductor chip onto a support by way of the cut piece of the die bonding resin layer in close contact with the rear face thereof, so as to obtain the semiconductor devices.

Kajiyama discloses attaching an expandable holding member (9) to the rear face (20b) of the semiconductor substrate by way of a die bonding resin layer (6, adhesive polyimide resin) (fig. 5 & 7); cutting the die bonding resin layer along each of cut surfaces of the semiconductor chips by expanding the holding member after attaching the holding member (fig. 9), so as to obtain the semiconductor chips each having the front face formed with the function device and having a cut piece of the die bonding

resin layer in close contact with the rear face thereof (fig. 10) in order to easily remove the semiconductor chips from the expandable holding member (9) by expanding the expandable holding member that reduces the adhesion between the expandable holding member and the die bonding resin layer.

Regarding mounting the semiconductor chip onto a support body, it is conventional in the art to mount the individual/singulated semiconductor chip onto the support body such as a heat dissipation plate, a lead frame, or a printed circuit board so as to reduce the heat from the semiconductor chips and/or to proceed to the packaging process of the semiconductor chip as evidenced by Swada disclosing that the element is mounted onto the lead frame (fig. 13C-D and paragraph 4,12).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Kurosawa with that of Kajiyama so that to easily remove the semiconductor chips from the expandable holding member and with that of Swada so as to reduce the heat from the semiconductor chips and/or to proceed to the packaging process of the semiconductor chip.

Re Claim 10, Swada teaches that wherein the support body is a lead frame (R, paragraph 12).

Re Claim 11, Kajiyama teaches wherein the holding member is expanded after the protective member is removed from the front face of the semiconductor substrate (fig. 7-9).

4. **Re Claim 12**, Kurosawa teaches a method for manufacturing a semiconductor device having a front face formed with a plurality of functional devices into the individual functional devices, so as to manufacture a semiconductor device having the functional device, the method comprising the steps of:

attaching a protective member (22) to the front face (21A) of the semiconductor substrate (21), such that the functional devices (21-1,21-2,21-3) are covered (fig. 16);

irradiating the semiconductor substrate with laser light (29) while position a light-converging point (a point where the light converges) within the semiconductor substrate with a rear face (21B) of the semiconductor substrate acting as a laser light incidence face after attaching the protective member (fig. 21), so as to form a modified region (30A-1,30A-2,30A-3), and causing the modified region to form a starting point region (col. 4, lines 64-67) for cutting along each line along which the semiconductor substrate should be cut, the lines set like a grid running (fig. 21, dotted lines) between the neighboring functional devices, inside by a predetermined distance from the laser light incidence face (fig. 21, see distance from the rear surface and the modified regions);

attaching an expandable holding member (26) to the rear face (21B) of the semiconductor substrate after forming the starting point regions for cutting (fig. 21, 26); and

cutting the semiconductor substrate into a plurality of semiconductor chips from the starting point regions for cutting along each of the lines in the grid (fig. 25-26).

However, Kurosawa does not disclose attaching an expandable holding member is by way of a die bonding resin layer; cutting the die bonding resin layer along each of

cut surfaces of the semiconductor chips by expanding the holding member after attaching the holding member, so as to obtain the semiconductor chips each having the front face formed with the function device and having a cut piece of the die bonding resin layer in close contact with the rear face thereof; and mounting the semiconductor chip onto a support by way of the cut piece of the die bonding resin layer in close contact with the rear face thereof, so as to obtain the semiconductor devices.

Kajiyama discloses attaching an expandable holding member (9) to the rear face (20b) of the semiconductor substrate by way of a die bonding resin layer (6, adhesive polyimide resin) (fig. 5 & 7); cutting the die bonding resin layer along each of cut surfaces of the semiconductor chips by expanding the holding member after attaching the holding member (fig. 9), so as to obtain the semiconductor chips each having the front face formed with the function device and having a cut piece of the die bonding resin layer in close contact with the rear face thereof (fig. 10) in order to easily remove the semiconductor chips from the expandable holding member (9) by expanding the expandable holding member that reduces the adhesion between the expandable holding member and the die bonding resin layer.

Regarding mounting the semiconductor chip onto a support body, it is conventional in the art to mount the individual/singulated semiconductor chip onto the support body such as a heat dissipation plate, a lead frame, or a printed circuit board so as to reduce the heat from the semiconductor chips and/or to proceed to the packaging process of the semiconductor chip as evidenced by Swada disclosing that the element is mounted onto the lead frame (fig. 13C-D and paragraph 4,12).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Kurosawa with that of Kajiyama so that to easily remove the semiconductor chips from the expandable holding member and with that of Swada so as to reduce the heat from the semiconductor chips and/or to proceed to the packaging process of the semiconductor chip.

Re Claim 13, Swada teaches that wherein the support body is a lead frame (R, paragraph 12).

Re Claim 14, Kajiyama teaches wherein the holding member is expanded after the protective member is removed from the front face of the semiconductor substrate (fig. 7-9).

Response to Arguments

5. Applicant's arguments with respect to amended claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL WHALEN whose telephone number is (571)270-3418. The examiner can normally be reached on Monday-Friday, 8:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. W./
Examiner, Art Unit 2829
04/16/2009

Daniel Whalen
/Michael S. Lebentritt/

Primary Examiner, Art Unit 2829